C-Band GaAs MMIC Limiting Power Amplifier with Small Insertion Phase Variation

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ABSTRACT

A C-band GaAs MMIC limiting power amplifier has been developed by cascading three kinds of MMIC chips (a limiting amplifier, a gain-control amplifier and a power amplifier) in a single package. It provides an output power of 33.2 $\pm$ 0.2 dBm with an insertion phase variation of less than 2.3 degrees over an input power range of from 13.5 dBm to 18.5 dBm. The output power can be controlled between 17.8 dBm and 33.2 dBm with an insertion phase variation less than 22.5 degrees.

INTRODUCTION

Transmitters for microwave communication systems often require an amplifier with power limiting and output power control capabilities with a small insertion phase variation.

For achieving such requirement, we have developed a C-band GaAs MMIC limiting power amplifier with a small insertion phase variation in C-band. The amplifier is realized by cascading three kinds of MMIC chips; a single-stage FET limiting amplifier, a single-stage dual-gate FET gain-control amplifier and a two-stage 2-W power amplifier.

Previously reported MMIC limiters have employed the combination of Schottky diode limiters and amplifiers [1],[2]. These diode limiters do not provide sharp limiting action due to series resistance of Schottky diode employed in MMICs. Furthermore, the multi-stage configuration makes chip size large [2]. In order to realize a limiting amplifier in a compact size with desired performance, we have employed an FET limiting amplifier configuration.

The developed MMIC limiting power amplifier provides an output power of 33.2 $\pm$ 0.2 dBm with an insertion phase variation of less than 2.3 degrees over an input power range of from 13.5 dBm to 18.5 dBm. The output power can be controlled between 17.8 dBm and 33.2 dBm. This paper reports the design, fabrication and measured results of the amplifier.

CIRCUIT DESIGN

A. Limiting Amplifier

Fig. 1 shows the equivalent circuit of the MMIC limiting amplifier. For stable operation, a resistive feedback configuration is employed. Since the drain of FET is biased through a resistor, the drain-source voltage V_{DS} changes according to the drain current I_{DS}. With an increase of RF input power, I_{DS} increases due to the rectification when the gate is biased near pinch-off. Accordingly V_{DS} decreases due to the voltage drop across the biasing resistor, and the output power is limited to an appropriate level. Since the gate-source capacitance of FET changes only slightly in the operating bias condition, the insertion phase variation can be kept small.

The FET used in the MMIC has a gate width of 800 μ m. Input and output matching networks have been optimized experimentally for minimizing output power

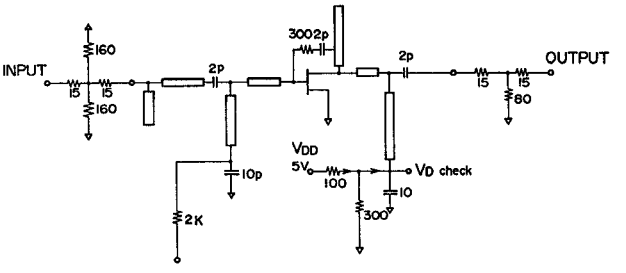

Fig. 1. Equivalent circuit of limiting amplifier.

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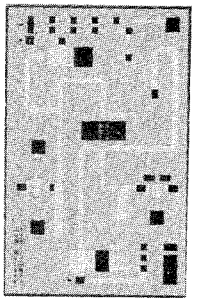

Fig. 2. MMIC limiting amplifier chip.

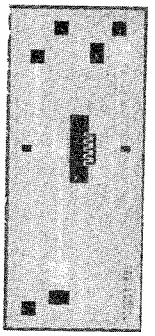

Fig. 4. MMIC gain control amplifier chip.

and insertion phase deviation against input power. Since the limiting characteristics are found sensitive to the matching condition, 5-dB attenuators are inserted at the input and output ports, respectively. The limiting amplifier is designed for obtaining an output power of 6 dBm over an input power range of 16.0 ± 2.5 dBm.

Fig. 2 shows the top view of the limiting amplifier chip which has a size of 1.9 × 3.0 mm.

B. Gain Control Amplifier

The MMIC gain control amplifier has been realized by using a dual-gate FET. The equivalent circuit is shown in Fig. 3. The control voltage is applied through the resistors to the second gate. The terminating impedance for the second gate is determined to minimize the insertion phase variation accompanying gain control and also to achieve the amplifier stability [3]. The gate width of the FET is selected to be 2.0 mm to achieve the output power of 17 dBm. The input and output matching networks are optimized in terms of gain and VSWR. The simulation of the amplifier shows a gain of more than 15 dB and a gain control of more than 10 dB for the control voltage of from 0 V to -5 V.

Fig. 4 shows the gain control amplifier chip. The chip size is 1.4 × 3.3 mm.

C. Power Amplifier

Fig. 5 shows the equivalent circuit of the two-stage MMIC power amplifier. In order to realize a small insertion phase variation for an output power of up to 2

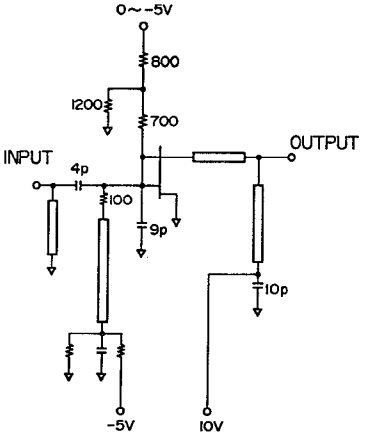

Fig. 3. Equivalent circuit of gain control amplifier.

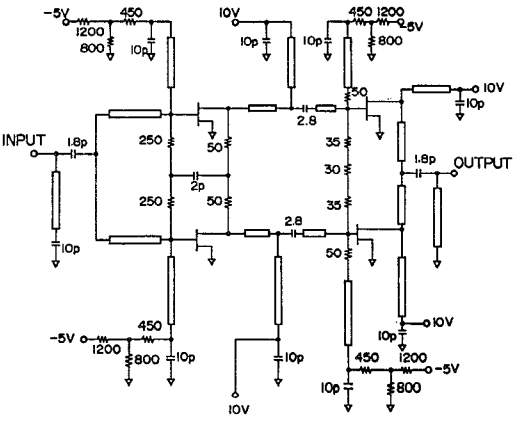

Fig. 5. Equivalent circuit of two-stage power amplifier.

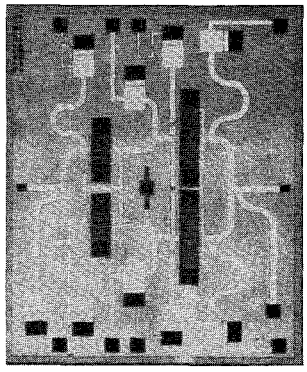

Fig. 6. MMIC power amplifier chip.

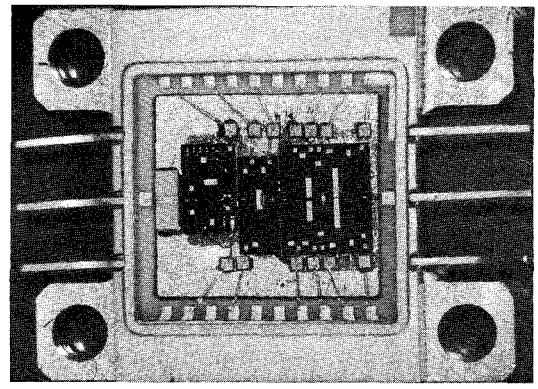

Fig. 7. MMIC limiting power amplifier.

W, the amplifier is designed to deliver an output power of more than 3 W for operating in linear region. The gate widths of FETs are 4.0 mm for the first stage and 8.0 mm for the second stage. A resistive feedback configuration is employed in the first stage in order to improve the stability and bandwidth [4]. The matching circuit has been optimized in terms of bandwidth, power, gain and VSWR. The amplifier simulation gives a gain of more than 17 dB over a relative bandwidth of 20 % in C-band.

The top view of the power amplifier chip with a size of 3.1 × 3.7 mm is shown in Fig. 6.

FABRICATION

The FETs and resistors in the MMICs have been fabricated by using selective Si ion implantation into the undoped semi-insulating GaAs substrates. The FETs have designed to have a gate length of 0.7 μ m. Via-holes for grounding have been formed by reactive ion etching (RIE). SiN film with a thickness of 300 nm is used for MIM capacitor dielectric. The thickness of all MMIC substrates is 100 μ m.

MEASURED RESULTS

The MMIC limiting power amplifier has been realized by cascading the limiting amplifier chip, the gain control amplifier chip and the power amplifier chip. The chips are mounted in a single ceramic package as shown in Fig. 7.

Fig. 8 shows the measured input-output RF power characteristic at a certain frequency f_0 in C-band at a control voltage V_C of 0 V. The supplied drain

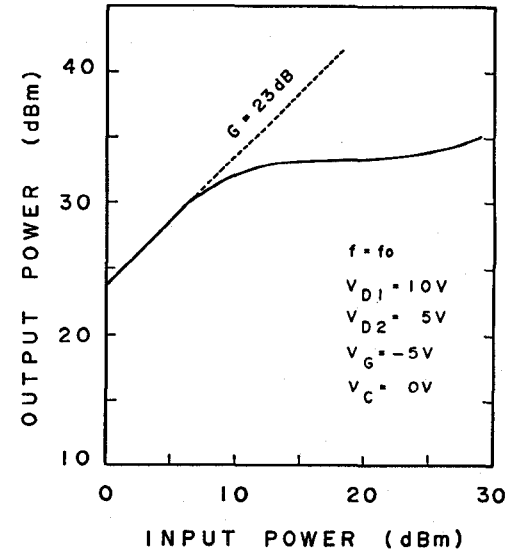

Fig. 8. Measured output power vs. input power of MMIC limiting power amplifier.

voltage for the gain control amplifier and power amplifier V_{D1} and for the limiting amplifier V_{D2} and gate voltage for all amplifiers V_G are designed to be 10 V, 5 V and -5 V, respectively. A small signal gain of 23 dB and an output power at 1-dB gain compression point of 31.5 dBm have been obtained. It can be seen that the limiting power amplifier exhibits power limiting for an input power variation of more than 15 dB.

Fig. 9 shows the measured output power over an input power range of from 13.5 dBm to 18.5 dBm at f_0. At a control

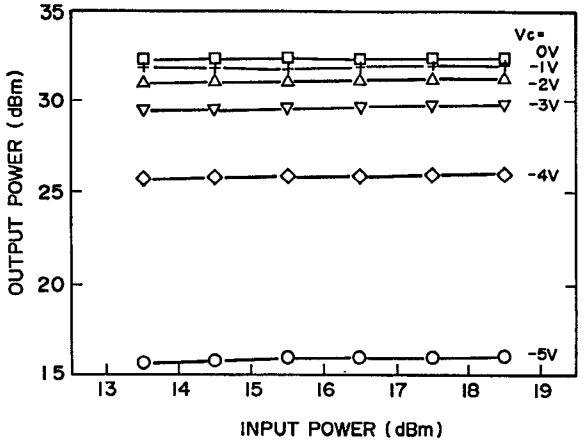

Fig. 9. Measured output power vs. input power of MMIC limiting power amplifier under power limiting operation.

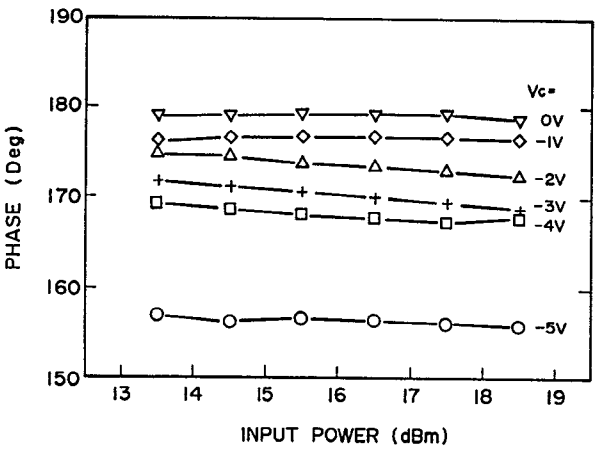

Fig. 10. Measured insertion phase vs. input power of MMIC limiting power amplifier under power limiting operation.

voltage of 0 V, the limiting power amplifier provides an output power of 33.2 ± 0.2 dBm over the input power range shown. The output power can be controlled down to as low as 17.8 dBm by setting the control voltage at -5 V.

Fig. 10 shows the measured insertion phase against the RF input power. An insertion phase variation of less than 2.3 degrees has been obtained over an input power range of 16.0 ± 2.5 dBm at the control voltage of 0 V. The insertion phase variation accompanying power control is less than 22.5 degrees over the output power range of from 17.8 dBm to 33.2 dBm.

CONCLUSION

It has been shown that the GaAs MMIC limiting power amplifier exhibits a small insertion phase variation both in the power limiting mode and the power control mode. Though the present amplifier consists of three chips of different functions, trade-offs are presently being made in terms of yield and cost to decide the feasibility of one-chip configuration.

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